IN THE CLAIMS

Please cancel claims 11-13 and 18, and amend the claims as follows:

1. (Currently amended) A process for fabricating a solid, large area platform mounted in a cavity in a wafer and supported for motion with respect to the wafer by integral, flexible, supports, comprising:

producing on a top surface of the wafer a first pattern defining the size, shape and location of ~~a~~ the large area platform[[,]] and ~~actuators~~ the supports for the platform;

etching through said first pattern to produce in a top portion of the wafer top surface trenches surrounding mesas corresponding to said platform[[,]] and said supports ~~and said actuators~~;

producing on a bottom surface of the wafer a second pattern corresponding to the size, shape and location of said platform;

etching through said second pattern to produce in a bottom portion of the wafer a bottom trench corresponding to said platform, the bottom trench being aligned with but spaced below the top trench surrounding the mesa corresponding to said platform;

further etching the top trenches to cause the top surface trench surrounding the mesa corresponding to said platform to intersect said bottom trench to produce a though trench to free said platform; and

additionally etching said top trenches to undercut said mesas to release said supports ~~and said actuators~~ from the wafer underlying the supports ~~and actuators~~, the ends of said supports being integral with and cantilevered from the wafer and the platform and extending therebetween to support the platform.

2. (Original) The process of claim 1, wherein producing said first pattern on the top surface of a wafer includes coating the top surface with an oxide layer, and photolithographically patterning said oxide layer.

3. (Original) The process of claim 2, wherein etching through said first pattern includes performing a silicon etch using a high etch rate high selectivity reactive ion etch.

4. (Original) The process of claim 3, wherein said etching includes alternate etch and passivation cycles.

5. (Original) The process of claim 1, wherein producing a second pattern on a bottom surface of said wafer includes coating the bottom surface with a second oxide layer and photolithographically patterning said second oxide layer.

6. (Original) The process of claim 5, wherein patterning said second oxide layer includes aligning a bottom surface pattern with the pattern produced on said top surface.

7. (Original) The process of claim 5, wherein etching through said second pattern includes performing a second silicon etch which extends into said wafer and stopping said second silicon etch before it reaches said top surface trenches.

8. (Original) The process of claim 1, wherein further etching includes deepening said top surface trenches to intersect said bottom trench.

9. (Original) The process of claim1, wherein additionally etching said top trenches includes an isotropic silicon release etch.

10. (Currently amended) The process of claim 1, further including sputter coating said large area platform, and said flexible supports and said actuators with a conductive material.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Original) A process for fabricating a micromechanical device comprising:

producing a first pattern on the top surface of a substrate;

etching said pattern to form a first trench in the substrate with a depth of less than twenty (20) percent of the substrate thickness:

producing a second pattern on the bottom surface of the substrate;

etching said second pattern to form a second trench in the substrate with a depth which is less than the thickness of the substrate minus the depth of the trench formed from the top surface:

further etching said top surface trench to cause the bottom of said first trench to intersect with said second trench.

15. (Original) The process of claim 14, wherein said etching is accomplished by reactive ion etching techniques.

16. (Original) The process of claim 14, wherein said substrate is a silicon wafer.

17. (Original) The process of claim 14, wherein the step of etching said pattern to form said first trench includes etching to a depth of between 20 and 50 microns.

18. (Cancelled)

19. (Currently amended) A process for fabricating a micromechanical device comprising;

producing a first pattern on the top surface of a substrate;

etching said pattern to form a plurality of top trenches in the substrate with a depth of less than ~~two~~ twenty (20) percent of the substrate thickness;

producing a second pattern on the bottom ~~of the~~ surface of the substrate, said second pattern being aligned with the top surface pattern ~~such~~ so that at least one structure defined by said second pattern lies directly opposite at least one trench formed from the top surface;

etching said second pattern to form a bottom trench in the substrate with a depth which is less than the thickness of the substrate minus the depth of the trench formed from the top surface;

further etching said top surface trenches to cause lateral etching in at least one pair of adjacent trenches to ~~overlap~~ undercut and thereby release the structure between them, and to cause vertical etching of the bottom of at least one top trench to cause it to intersect with the bottom trench previously formed by etching from the bottom surface.

20. (Currently amended) A process for fabricating a solid, large area platform mounted in a cavity in a wafer ~~for motion with respect to the water~~ by integral, flexible supports, comprising:

producing on a top surface of the wafer a first pattern defining the size, shape and location of a large area platform, supports for the platform, and electrodes for the platform;

etching through said first pattern to produce in a top portion of the wafer top surface trenches surrounding mesas corresponding to said platform, said supports and said electrodes;

depositing a protective layer on said mesas, the walls of said trenches and the bottom surfaces of said trenches;

producing on a bottom surface of the wafer a second pattern corresponding to the size, shape and location of said platform and vertically aligned with said first pattern;

etching through said second pattern to produce in a bottom portion of the wafer a bottom trench corresponding to said platform, the bottom trench being aligned with but ~~space~~ spaced below the top trench surrounding the mesa corresponding to said platform;

removing the protective layer from the bottom surfaces of the top trenches; and

further etching the top trenches vertically to cause the top surface trench ~~surround~~ surrounding the mesa corresponding to said platform to intersect said bottom trench to produce a through trench to free said platform, and to horizontally undercut said mesas to release said supports and said electrodes from the wafer underlying the supports and electrodes, the ends of said supports being integral with and cantilevered from the wafer and the platform and extending therebetween to support the platform.

21. (Original) The process of claim 20, wherein producing said first and second pattern includes coating the wafer with an oxide layer and producing said pattern in said oxide layer by photolithography and etching.

22. (Original) The process of claim 20, wherein said etching of trenches includes performing silicon etching by reactive ion etching techniques.

23. (Original) The process of claim 20, further including depositing electrically conductive material on the top surfaces of said platform, said supports and said electrodes.

24. (New) The process of claim 14, further including isotropically ion etching said top surface trench to undercut the top surface of said trench to produce released cantilevered structures connected to said substrate.

25. (New) The process of claim 24, wherein producing said first and second patterns includes defining aligned trenches surrounding a large are a platform to be formed in a cavity in said substrate.

26. (New) The process of claim 25, wherein producing said first and second patterns includes defining said cantilevered support structures, to extend between said substrate and said platform.

27. (New) A process for fabricating a large area, solid microelectromechanical platform supported by released, integral, flexible supports, comprising:

etching the top side of a wafer to form top trenches defining the platform and supports connected to the platform;

etching the bottom side of the wafer to form bottom trenches aligned with the top trenches;

further etching from the top side of the wafer to connect the trenches defining the platform to free the platform; and

laterally underetching the supports to release them, thereby enabling the platform to move with respect to the wafer.

28. (New) The process of claim 27, wherein the step of includes isotropic ion etching.

29. (New) The process of claim 27, wherein etching the top side and the bottom side of the wafer includes etching around the defined platform for producing a platform having a thickness substantially equal to the thickness of the wafer.

30. (New) The process of claim 27, wherein etching the bottom side of the wafer includes widening the bottom surface trench to etch a portion of the bottom surface of the defined platform to produce a thinned platform.

31. (New) The process of claim 27, wherein etching the bottom trenches includes timing the etch to ensure that the platform is not freed during the bottom etching.

32. (New) The process of claim 27, wherein further etching from the top surface includes performing a trench etch to deepen the first-formed trenches.

33. (New) The process of claim 32, wherein laterally underetching includes performing an isotropic release etch in the trenches to create cantilevered supports extending between the platform and the wafer.